a first multiplexer having inputs coupled to outputs of the plurality of latches and which recombines the incoming data bits into the original sequence;

a decode gating circuit [[also]] coupled to the outputs of the plurality of latches and configured to identify when the pre-set sequence of digital bits is received at the activate circuit; and

a delay circuit, which receives one or more outputs from the decode gating circuit and which generates one or more delayed outputs.

22. (currently amended) The data communication system of Claim 21, further comprising:

a time adjust system, which receives the one or more delayed outputs from the delay circuit and an output from the first multiplexer, and which adjusts selective combinations of the one or more delayed outputs and the [[said]] output from the first multiplexer by a pre-set number of delay bit periods to produce [[a]] the test [[output]] data.

23. (currently amended) The data communication system of Claim 22, further comprising:

a second multiplexer having:

a first input coupled to the output of the first multiplexer for receiving serial data transmitted through the activate circuit for normal operation;

a second input coupled to the test [[output]] data of the time adjust system for receiving test data during test operation; and

a control input at which jitter is introduced into the communication system, wherein the second multiplexer selectively outputs one of the serial data and the test data depending on the control input.

24. (previously presented) The data communication system of Claim 23, further comprising:

an optical cable drive assembly coupled to an output of the second multiplexer and which receives an output selected by the control input from the second multiplexer.

25. (previously presented) The data communication system of Claim 24, wherein:

the data communication system is a station within a fiber optic network, further comprising a fiber optic subassembly for interfacing with a fiber channel; and

the optical cable drive assembly comprises:

a first optical drive assembly providing a wrap path to a receive logic of the data communication system; and

a second optical drive assembly providing data output to the fiber channel.

26. (previously presented) The data communication system of Claim 25, wherein the random digital sequence generator comprises a linear feedback shift register.